NEX81915

Fast turn-off dual synchronous rectifiers (SR) controller

Rev. 1.2 — 17 September 2025 Product data sheet

1. General description

NEX81915 is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It supports operation in discontinuous conduction mode (DCM), continuous conduction mode (CCM) and critical conduction mode (CRM). It has two driver stages for driving the SR MOSFETs. By detecting the V_{ds} of the rectifier, the MOSFETs can be reliably switched on and off, thereby replacing Schottky diodes and improving the efficiency of the resonant converter.

NEX81915 regulates the forward drop voltage of an external synchronous rectifier (SR) MOSFET by decreasing the gate voltage. This allows the SR FET to be turned off quickly when the V_{ds} becomes positive.

NEX81915 is a green and energy-saving product. The turn-on delay time will be increased and the drive current will be decreased to minimize the power consumption at light load. The IC current will drop to a very low level during burst off period. The light load efficiency can be improved.

The device is available in SO8 (SOT96-2) package.

2. Features and benefits

- 120 V voltage rating support maximum 48 V output
- Supports CCM, CRM and DCM operation
- Works with Standard and Logic level MOSFETs
- Wide supply voltage ranges from 4.7 V to 35.0 V
- 140 µA low quiescent current in light load mode
- Regulation level of -37 mV for driving low-ohmic MOSFETs
- Adaptive gate drive for fast turn-off at the end of conduction
- Interlock function for channel A and B
- Available in an SO8 package
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V

3. Applications

- AC/DC adapters
- PC power supplies
- LCD TV power supplies
- Isolated DC-DC power converters

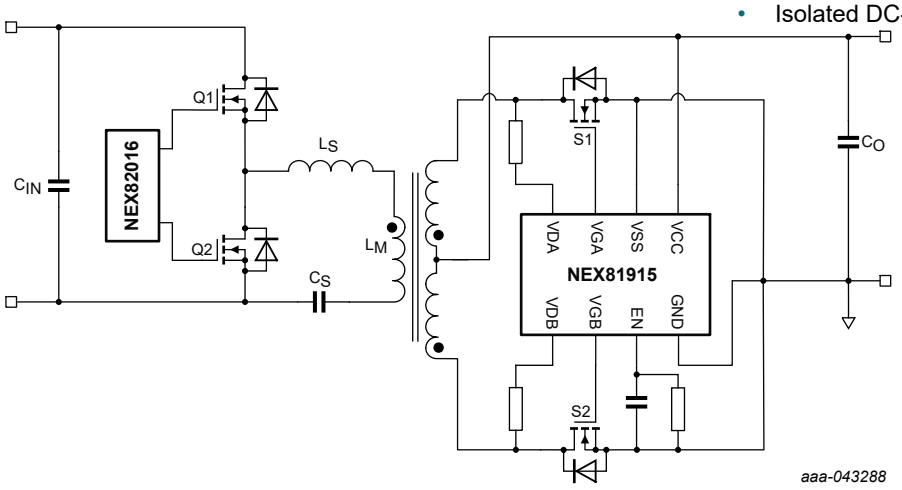


Fig. 1. Typical application circuit

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range (T_j)	Name	Description	Version
NEX81915D	-40 °C to 125 °C	SO8	Plastic, small outline package; 8 leads; 1.27 mm pitch; 4.90 mm x 3.90 mm x 1.75 mm body	SOT96-2

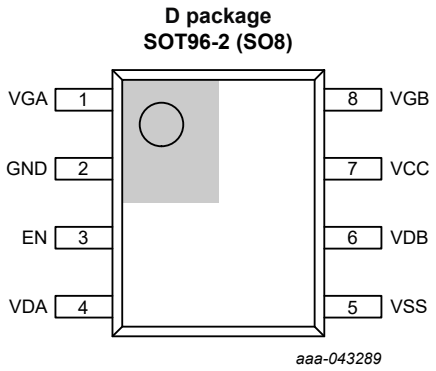
5. Marking

Table 2. Marking code

Type number	Marking code
NEX81915D	N81915

6. Pinning information

6.1. Pinning configuration



6.2. Pin description

Symbol	Pin	Description
VGA	1	gate driver output for channel A
GND	2	IC power ground
EN	3	if the voltage is less than 0.35 V, enter the disable mode
VDA	4	drain sense input for channel A
VSS	5	used as reference for VDA and VDB voltage sampling
VDB	6	drain sense input for channel B
VCC	7	IC power supply up to 35 V
VGB	8	gate driver output for channel B

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	VCC to GND		-0.3	38.0	V
V_{SS}	VSS to GND		-0.3	0.3	V
V_{GA}, V_{GB}	VGA, VGB to GND		-	20	V
V_{DA}, V_{DB}	VDA, VDB to GND		-	120	V
P_{tot}	total power dissipation	T_{amb} = 75 °C	-	0.8	W
T_j	operation junction temperature		-40	150	°C
T_{stg}	storage temperature		-55	150	°C
T_{lead}	lead temperature (10 s)		-	260	°C

[1] Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Section 10. Exposure to these limiting values for extended periods may affect device reliability.

8. ESD ratings

Table 4. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	-	2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	-500	-	500	V

9. Thermal characteristics

Table 5. Thermal characteristics

For more information about thermal metrics, consult the application note.

Symbol	Parameter	SOT96-2	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	90	°C/W
$R_{\Theta JC}$	junction-to-case (bottle) thermal resistance	45	°C/W

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to VS (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	VCC to GND		4.7	35.0	V
T_j	operation junction temperature		-40	125	°C

11. Electrical characteristics

Table 7. Electrical characteristics

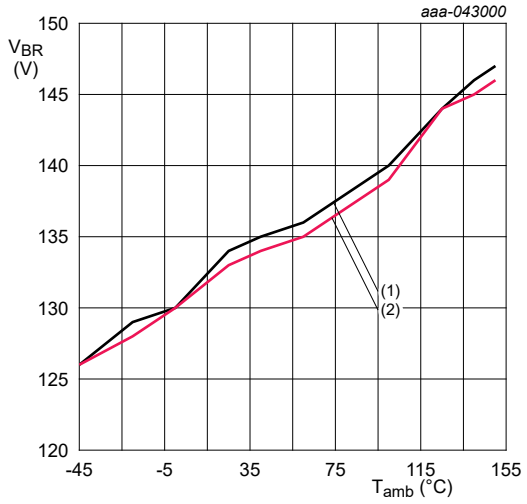
Where V_{CC} = 4.8 V to 35.0 V; typical values are measured at V_{CC} = 12 V; T_j = 25 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply pin (VCC)						
V_{CC_range}	VCC voltage range		4.7	-	35.0	V
V_{CC_ON}	VCC UVLO rising		4.3	4.5	4.7	V
V_{CC_HYS}	UVLO hysteresis		0.20	0.25	0.30	V
I_{CC}	VCC operating current	C_{Load} = 4.7 nF; F_{sw} = 100 kHz	8.0	12.5	17.0	mA
I_Q	VCC quiescent operation current	IC enable without gate driver	1.8	2.3	2.8	mA
I_{LL}	light load mode current	under light load mode	110	140	170	µA
Control circuitry (VDA; VDB; VSS)						
V_{th_on}	turn-on threshold	V_{CC} = 12 V	-260	-230	-200	mV
V_{th_off2}	V_{ds} regulation threshold		-44	-38	-32	mV
V_{th_off}	turn-off threshold		28	36	44	mV
$V_{th\text{-}b}$	turn-off threshold	enabled after t_{bon}	1.6	2.0	2.4	V
t_{don}	turn-on delay at heavy load	$t_{LL} < t_{LL\_EXIT}$	80	110	140	ns
t_{bon}	turn-on blanking time	C_{Load} = 4.7 nF	0.3	0.6	0.9	µs
t_{boff}	turn-off blanking time	C_{Load} = 4.7 nF	1.2	1.5	1.8	µs
$t_{interlock}$	interlock time	[1]	-	200	-	ns
Light load control						
$t_{LL\text{-}ENT}$	entry time for light load		34.5	45.0	56.5	µs
$t_{LL\text{-}EXIT}$	exit time for light load		-	1	-	cycle
Gate driver						
V_{G_H}	VG (high)	V_{CC} = 12 V to 35 V	10.0	11.5	13.0	V
V_{G_L}	VG (low)	VG sink = 100 mA	0.035	0.060	0.085	V
I_{source}	maximum source current	[1]	-	200	-	mA
$R_{pd(sink)}$	pull-down impedance	VG sink = 100 mA	0.35	0.60	0.85	Ω
$t_{D\text{-}gateoff}$	turn-off total delay	V_{DA} = V_{SS}; C_{Load} = 1 nF; R_{GATE} = 0 Ω; V_{GS} = 2 V	-	35	60	ns
		V_{DA} = V_{SS}; C_{Load} = 4.7 nF; R_{GATE} = 0 Ω; V_{GS} = 2 V	-	45	80	ns
In-chip OTP						
T_{OTP}	OTP enter	[1]	145	160	175	°C
T_{OTP_HYS}	hysteresis for OTP exit	[1]	10	20	30	°C

[1] Guaranteed by design.

12. Typical characteristics

Table 8. Typical characteristics



(1) V_{DA}

(2) V_{DB}

Fig. 2. Breakdown voltage vs. temperature

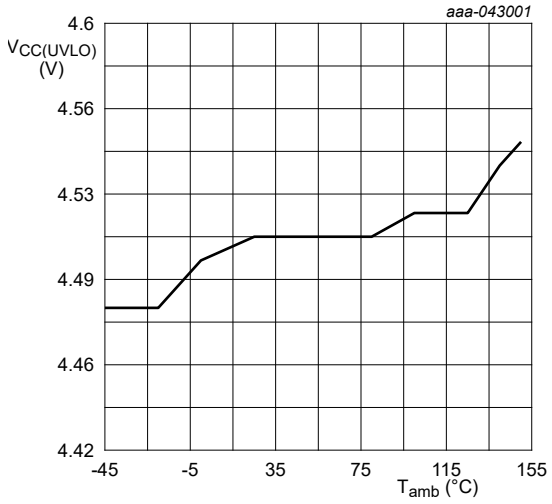
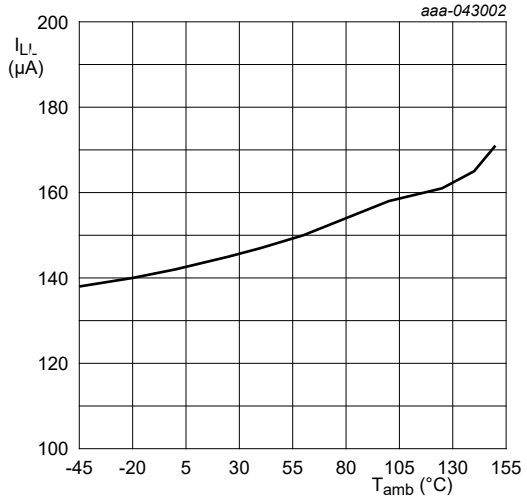
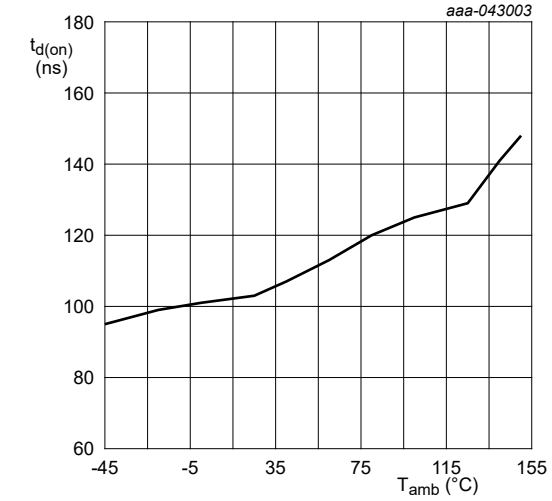


Fig. 3. $V_{CC\ UVLO\ (OFF)}$ vs. temperature



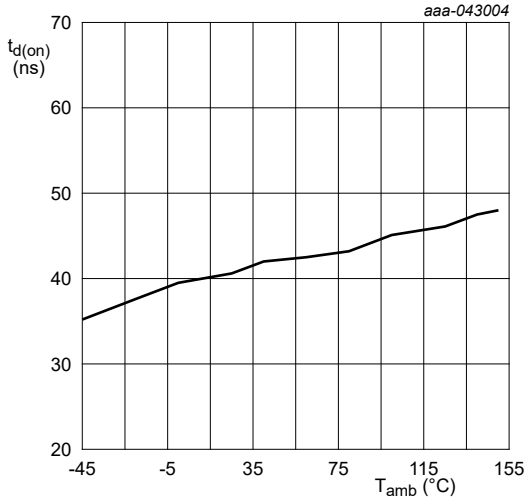
V_{CC} = 24 V

Fig. 4. Light-load mode current vs. temperature



C_{Load} = 1 nF

Fig. 5. Turn-on delay vs. temperature



C_{Load} = 4.7 nF

Fig. 6. Turn-off delay vs. temperature

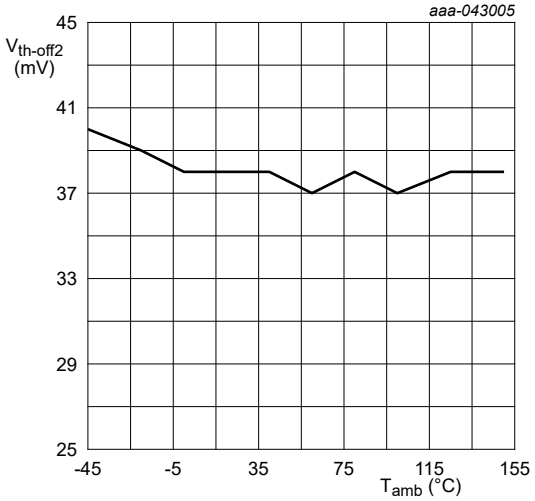


Fig. 7. V_{ds} regulation threshold vs. temperature

13. Detailed description

13.1. Overview

NEX81915 is a dual-channel controller on the second side of the resonant converter, which supports CCM, CRM and DCM operation, it automatically realizes optimal control under entire load range. NEX81915 has simple periphery and reliable protection. The following sections introduce its various functional modules in detail.

13.2. Functional block diagram

The NEX81915 functional block diagram is shown in Fig. 8:

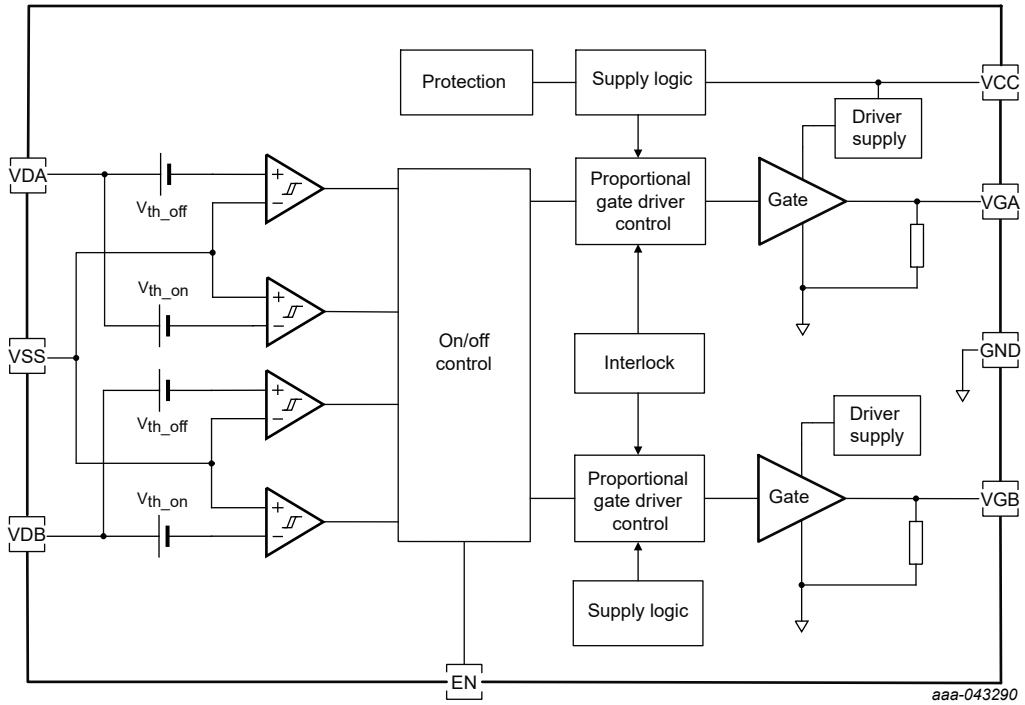


Fig. 8. Functional block diagram

13.3. Feature description

13.3.1. Start-up and under-voltage lockout (UVLO)

The maximum V_{CC} of NEX81915 is up to 35 V. The IC enters sleep mode and keeps the V_{GA} and V_{GB} low when V_{CC} is under UVLO threshold. The IC starts operating when V_{CC} rises above UVLO threshold.

13.3.2. MOSFET on/off control

Once the V_{ds} of MOSFET drops below V_{th_on}, the SR MOSFET will be turned on after a turn-on delay time, which is shown in Fig. 9.

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on-state lasts for a predetermined length of time. The default turn-on blanking time of NEX81915 is 0.9 µs.

When V_{ds} rises above V_{th_off2} (-37 mV), the gate voltage of the SR MOSFET will decrease to regulate V_{ds} at this threshold. When the V_{ds} turn-off threshold V_{th_off} (38 mV) is triggered, the SR MOSFET will be turned off very quickly because the gate voltage is very close to the MOSFET turn-off threshold.

During t_{bon} period, $V_{th\text{-}off}$ is adjusted to 90 mV to prevent false shutdown caused by circuit oscillation, while ensuring reliable shutdown of SR under extreme conditions to sustain safety.

The turn-off blanking timer starts when V_{ds} is higher than V_{th_off} threshold, the gate driver remains off for t_{boff}.

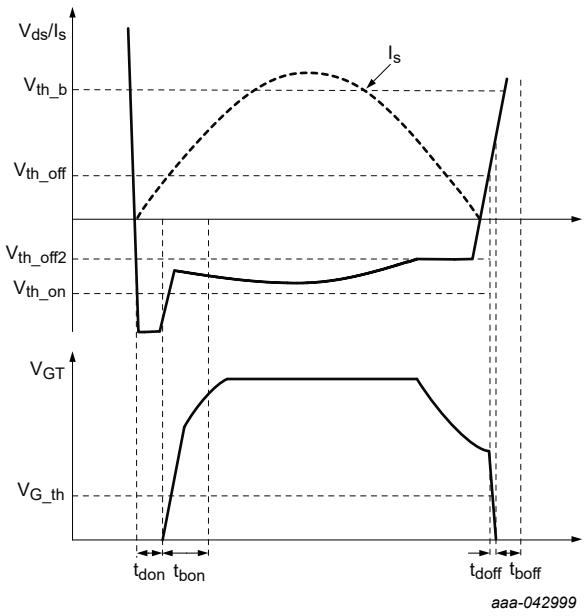


Fig. 9. Turn on/off timing

13.3.3. Burst-mode control

When the primary side controller operates in burst mode, NEX81915 will enter energy-saving mode, the turn-on delay time t_{don} will be increased and the drive current will be decreased to minimize the power consumption. This improves the light efficiency.

13.3.4. First on-cycle blanking

When the IC is enabled or exiting from energy-saving mode, the first switching cycle is shielded. This prevents the two MOSFETS from cross-conducting during the turn-on blanking time.

13.3.5. Channel interlock

NEX81915 incorporates an interlock function. The interlock function prevents two MOSFETs from conducting simultaneously. After turning off one MOSFET, the IC waits typically 200 ns ($t_{interlock}$) before turning on another MOSFET.

13.3.6. Thermal shutdown

When the junction temperature of the IC is higher than the over-temperature protection threshold, the driver will be shut down, and the IC will enter OTP mode. When the junction temperature decreases to typically 20 °C, the IC will exit OTP mode.

13.3.7. PCB layout guidelines

1. VDA and VDB respectively form two detection loops with VSS. VDA/VSS, VDB/VSS should be put as close as possible to each MOSFET (drain/source), the loop should be as small as possible. The two detection loops should be separated from each other with two independent small loops.
2. Place a decoupling capacitor with a minimum of 1 µF as close as possible between VCC and GND.

3. It is highly recommended to keep the sense loop away from the power loop. The sense loop and power loop can be placed on different layers to keep them separated from each other. Do not place the driver IC inside the power loop. This may affect MOSFET voltage sensing.
4. The VSS pin must be connected to the SR MOSFET source pin as close as possible. It minimizes voltage errors caused by parasitic inductance in combination with large di/dt.

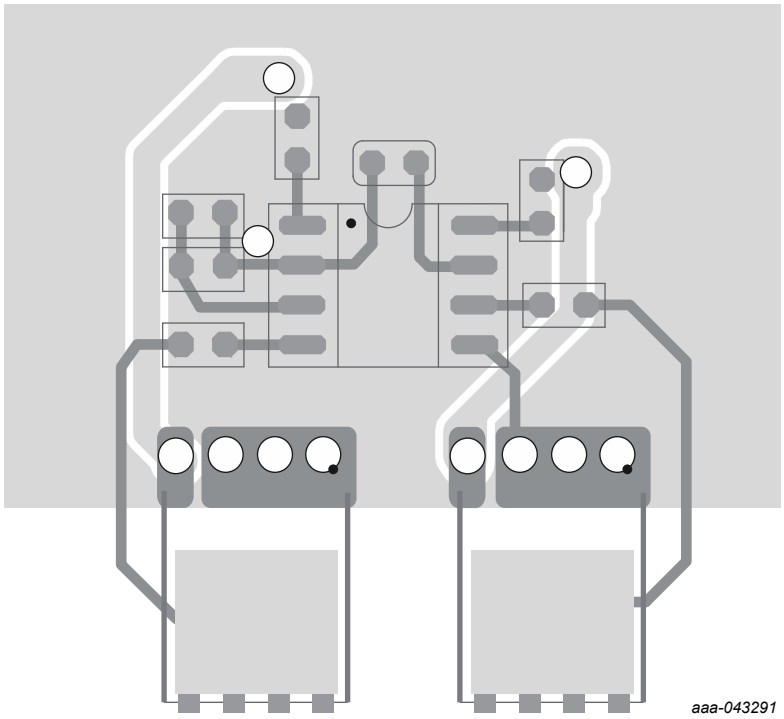
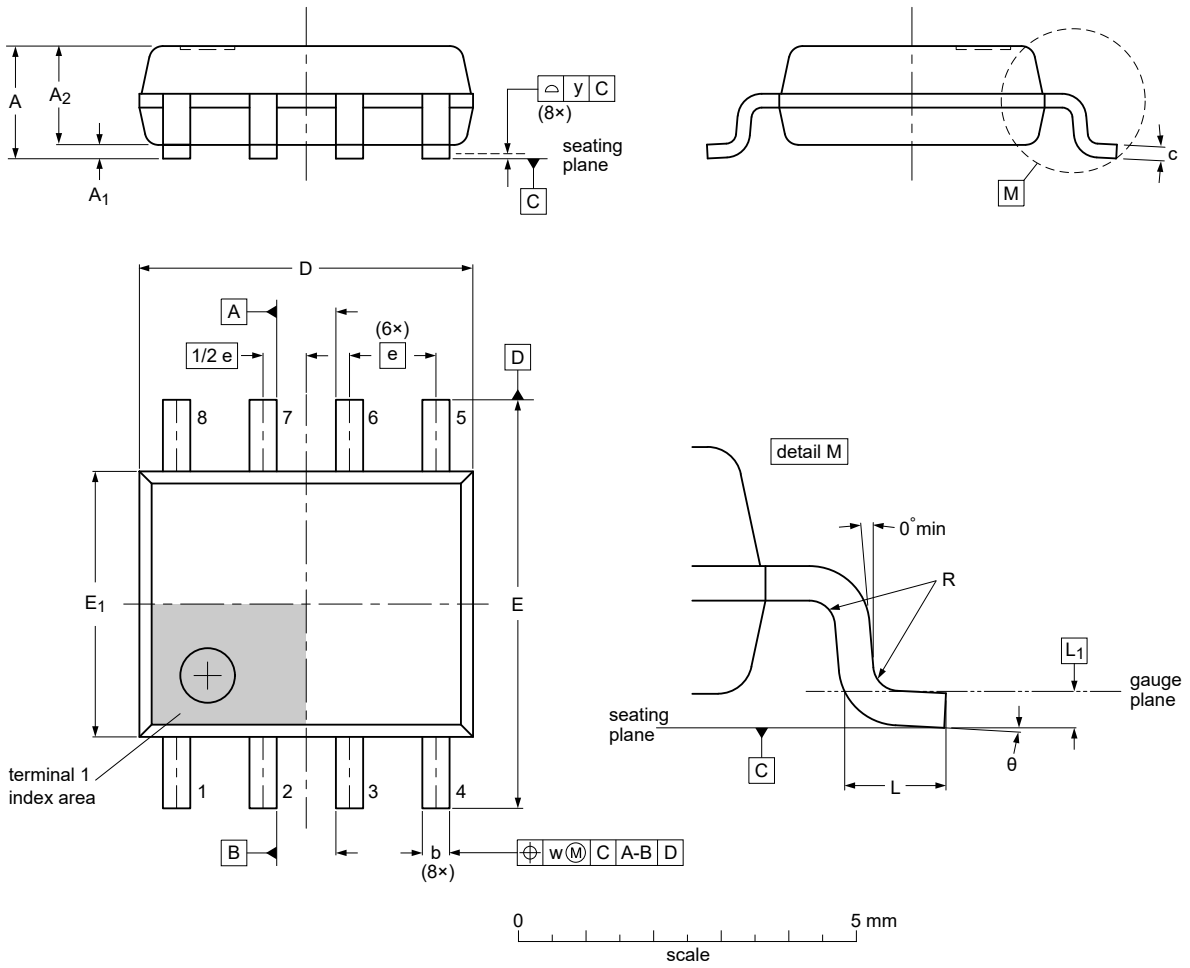


Fig. 10. Layout example

14. Package outline

Plastic, small outline package; 8 leads; 1.27mm pitch; 4.9 mm x 3.9 mm x 1.75mm body **SOT96-2**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	L	L_1	R	w	y	θ
mm	max	1.75	0.25	1.55	0.51	0.25	5.10	6.20	4.00	1.27 BSC	1.27	0.25 BSC	0.15 REF	0.25	0.10	8°
	nom															
	min	1.45	0.10	1.35	0.33	0.17	4.70	5.80	3.80		0.40					0°

Note

1. Dimension D does not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burr shall not exceed 0.15 mm per end. Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

sot96-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT96-2						25-03-12

Fig. 11. Package outline SOT96-2 (SO8)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CCM	Continuous Conduction Mode
CRM	Critical Conduction Mode
CDM	Charged Device Model
DCM	Discontinuous Conduction Mode
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
IC	Integrated Circuit
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
LCD	Liquid Crystal Display
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OTP	OverTemperature Protection
PC	Personal Computer
SR	Synchronous Rectifier
UVLO	Under-Voltage LockOut

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX81915 v. 1.2	20250917	Product data sheet	-	NEX81915 v. 1.1
Modifications:	• Section 1 and Section 2 updated. • Section 6.1: Package configuration drawing updated. • Table 6 and Table 7 updated. • Fig. 11: Package outline drawing updated.			
NEX81915 v. 1.1	20250905	Product data sheet	-	NEX81915 v. 1
Modifications:	• Fig. 11: Package outline drawing updated.			
NEX81915 v. 1	20250711	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 17 September 2025